(B) Starting on a separate page, appropriate remarks and arguments. 37 C.F.R. § 1.111 and MPEP 714; and

(C) Starting on a separate page, a marked-up version entitled: "Version with markings to show changes made."

Amendments

In the Claims:

Please add the following new claims:

54.(new) The method as recited in claim 1, wherein the first width and second width are each 64 bits.

55.(new) The method as recited in claim 54, wherein the third register is comprised of eight 8-bit elements.

56.(new) The method as recited in claim 54, wherein the third register is comprised of four 16-bit elements.

57.(new) The method as recited in claim 1, wherein the starting byte is specified as a variable in a register in an alignment instruction.

58.(new) The method as recited in claim 1, wherein the first vector and the second vector are in contiguous locations in the memory unit.

59.(new) The method as recited in claim 1, wherein the processor operates in a big-endian byte ordering mode.

60.(new) The method as recited in claim 1, wherein the processor operates in a little-endian byte ordering mode.

61.(new) The method as recited in claim 1, wherein the first vector and the second vector are each composed of eight 8-bit elements indexed from 0 to 7, and wherein said extracting step comprises:

extracting elements 4, 5, 6, and 7 from the first register.

62. (new) The method as recited in claim 61, wherein said replicating step comprises:

replicating an element 0 of the third register from an element 4 of the first register;

replicating, for all bits of an element 1 of the third register, a sign bit of the element 4 of the first register;

replicating an element 2 of the third register from an element 5 of the first register;

replicating, for all bits of an element 3 of the third register, a sign bit of the element 5 of the first register;

replicating an element 4 of the third register from an element 6 of the first register;

replicating, for all bits of an element 5 of the third register, a sign bit of the element 6 of the first register;

replicating an element 6 of the third register from an element 7 of the first register; and

replicating, for all bits of an element 7 of the third register, a sign bit of the element 7 of the first register.

63. (new) The method as recited in claim 1, wherein the first vector and the second vector are each composed of eight 8-bit elements indexed from 0 to 7, and wherein said extracting step comprises:

extracting elements 0, 1, 2 and 3 from the first register.

64. (new) The method as recited in claim 63, wherein said replicating step comprises:

replicating an element 0 of the third register from an element 0 of the first register;

replicating, for all bits of an element 1 of the third register, a sign bit of the element 0 of the first register;

replicating an element 2 of the third register from an element 1 of the first register;

replicating, for all bits of an element 3 of the third register, a sign bit of the element 1 of the first register;

replicating an element 4 of the third register from an element 2 of the first register;

replicating, for all bits of an element 5 of the third register, a sign bit of the element 2 of the first register;

replicating an element 6 of the third register from an element 3 of the first register; and

replicating, for all bits of an element 7 of the third register, a sign bit of the element 3 of the first register.